CLAIMS

1. An apparatus for providing a signal with an adjustable delay, comprising:

a delay line, having an input adapted to receive the signal, and including a plurality of taps outputting delayed versions of the signal;

a plurality of first stage multiplexers, the first stage multiplexers having inputs coupled to taps in the plurality of taps, and respectively providing signals from taps in the plurality of taps at respective first stage outputs selected in response to first stage control signals;

a second stage multiplexer having inputs coupled to the first stage outputs from the plurality of first stage multiplexers, and providing a signal from a selected tap at a second stage output in response to second stage control signals; and

logic generating the first and second stage control signals to select one of said plurality of taps as the selected tap, including, for all pairs of adjacent taps in the plurality of taps, logic to change the selected tap to the adjacent tap in the pair by switching only one of the first stage multiplexer or the second stage multiplexer.

2. The apparatus of claim 1, wherein the signal comprises a clock signal, and the delayed versions of the signal comprise phase shifted versions of the clock signal.

3. The apparatus of claim 1, wherein said delayed versions of the signal provided from adjacent taps differ in delay by less than 500 picoseconds.

4. The apparatus of claim 1, wherein said delayed versions of the signal provided from adjacent taps differ in delay by less than 200 picoseconds.

5. The apparatus of claim 1, wherein said delayed versions of the signal provided from adjacent taps differ in delay by an amount on the order of 100 picoseconds.

6. The apparatus of claim 1, wherein the signal comprises a clock signal having a frequency greater than 300 MHz, and the delayed versions of the signal comprises phase

shifted versions of the clock signal, and the phase shifted versions of the clock signal differ in phase by less than 200 picoseconds.

7. The apparatus of claim 1, wherein the delay line comprises a plurality of inverters in series, and the plurality of taps comprise buffers coupled to outputs of inverters in the plurality of inverters.

8. The apparatus of claim 1, wherein the logic comprises a first shift register and a second shift register, the output of the first shift register supplying the first control signals and the output of the second shift register supplying the second control signals.

9. The apparatus of claim 1, wherein the logic comprises a first bidirectional shift register and a second bidirectional shift register, the output of the first bidirectional shift register supplying the first control signals, the first control signals including a set of unselect bits and a select bit stored in the first bidirectional shift register corresponding with respective inputs of the first stage multiplexers, and the output of the second bidirectional shift register supplying the second control signals, the second control signals including a set of unselect bits and a select bit stored in the second bidirectional shift register corresponding with respective inputs of the second stage multiplexer; and

logic to shift unselect bits into the first bidirectional shift register from first and second directions to move the select bit for the first control signals, and to shift unselect bits into the second bidirectional shift register from first and second directions to move the select bit for the second control signals.

10. The apparatus of claim 1, wherein the logic comprises a first bidirectional shift register and a second bidirectional shift register, the output of the first bidirectional shift register supplying the first control signals, the first control signals including a set of unselect bits and a select bit stored in the first bidirectional shift register corresponding with respective inputs of the first stage multiplexers, and the output of the second bidirectional shift register supplying the second control signals, the second control signals

including a set of unselect bits and a select bit stored in the second bidirectional shift register corresponding with respective inputs of the second stage multiplexer; and

logic to shift unselect bits into the first bidirectional shift register from first and second directions to move the select bit for the first control signals, and to shift unselect bits into the second bidirectional shift register from first and second directions to move the select bit for the second control signals, including

when the select bit in the second control signals is in even positions in the second bidirectional shift register, shifting the unselect signals into the first bidirectional shift register from the same direction of the one of the first and second directions in which the unselect signals are shifted into the second bidirectional shift register, and when the select bit in the second control signals is in odd positions in the second bidirectional shift register, shifting the unselect signals into the first bidirectional shift register from the opposite direction of the one of the first and second directions in which the unselect signals are shifted into the second bidirectional shift register.

11. An apparatus for providing an output signal and an output clock signal with an adjustable phase, comprising:

a delay line, having an input adapted to receive a clock signal, and including a plurality of taps outputting phase shifted versions of the clock signal;

a plurality of first stage multiplexers, the first stage multiplexers having inputs coupled to taps in the plurality of taps, and respectively providing phase shifted versions of the clock signal from taps in the plurality of taps at respective first stage outputs selected in response to first stage control signals;

a second stage multiplexer having inputs coupled to the first stage outputs from the plurality of first stage multiplexers, and providing a selected phase shifted version of the clock signal from a selected tap at a second stage output in response to second stage control signals, as the output clock signal;

multiplexer logic generating the first and second stage control signals to select one of said plurality of taps as the selected tap in response to clock control signals, including, for all pairs of adjacent taps in the plurality of taps, logic to change the

selected tap to the adjacent tap in the pair by switching either the first stage multiplexers or the second stage multiplexer, but not both; and

logic to generate the clock control signals in response to relative timing of the output signal and the output clock signal.

12. The apparatus of claim 11, including:

a memory including memory cells, and having address/data paths and timing paths which emulate the address/data paths, the address/data paths outputting said output signal in response to addresses; and

an output clock phase detector coupled to the logic to generate the clock control signals and to the memory, which generates signals indicating the relative phase of transitions of the output signal and the output clock signal.

13. The apparatus of claim 11, including:

a memory including memory cells, and having address/data paths and timing paths which emulate the address/data paths, the address/data paths outputting data in response to addresses and the timing paths outputting dummy data in response to an address emulation signal;

an output clock phase detector coupled to the logic to generate the clock control signals and to the memory, which generates signals indicating the relative phase of transitions of the output signal and the output clock signal; and

delay locked loop, responsive to an input clock, to generate an address emulation signal on the timing paths in the memory.

14. The apparatus of claim 11, wherein said phase shifted versions of the clock signal provided from adjacent taps differ in phase by less than 500 picoseconds.

15. The apparatus of claim 11, wherein said phase shifted versions of the clock signal provided from adjacent taps differ in phase by less than 200 picoseconds.

16. The apparatus of claim 11, wherein said phase shifted versions of the clock signal provided from adjacent taps differ in phase by an amount on the order of 100 picoseconds.

17. The apparatus of claim 11, wherein the clock signal has a frequency greater than 300 MHz, and the phase shifted versions of the clock signal provided from adjacent taps differ in phase by less than 200 picoseconds.

18. The apparatus of claim 11, wherein the delay line comprises a plurality of inverters in series, and the plurality of taps comprise buffers coupled to outputs of inverters in the plurality of inverters.

19. The apparatus of claim 11, wherein the multiplexer logic comprises a first shift register and a second shift register, the output of the first shift register supplying the first control signals and the output of the second shift register supplying the second control signals.

20. The apparatus of claim 11, wherein the multiplexer logic comprises a first bidirectional shift register and a second bidirectional shift register,

the output of the first bidirectional shift register supplying the first control signals, the first control signals including a set of unselect bits and a select bit stored in the first bidirectional shift register corresponding with respective inputs of the first stage multiplexers, and

the output of the second bidirectional shift register supplying the second control signals, the second control signals including a set of unselect bits and a select bit stored in the second bidirectional shift register corresponding with respective inputs of the second stage multiplexer; with

logic to shift unselect bits into the first bidirectional shift register from first and second directions to move the select bit for the first control signals, and to shift unselect bits into the second bidirectional shift register from first and second directions to move the select bit for the second control signals.

21. The apparatus of claim 11, wherein the multiplexer logic comprises a first bidirectional shift register and a second bidirectional shift register,

the output of the first bidirectional shift register supplying the first control signals, the first control signals including a set of unselect bits and a select bit stored in the first bidirectional shift register corresponding with respective inputs of the first stage multiplexers, and

the output of the second bidirectional shift register supplying the second control signals, the second control signals including a set of unselect bits and a select bit stored in the second bidirectional shift register corresponding with respective inputs of the second stage multiplexer; with

logic to shift unselect bits into the first bidirectional shift register from first and second directions to move the select bit for the first control signals, and to shift unselect bits into the second bidirectional shift register from first and second directions to move the select bit for the second control signals, including

when the select bit in the second control signals is in even positions in the second bidirectional shift register, shifting the unselect signals into the first bidirectional shift register from the same direction of the one of the first and second directions in which the unselect signals are shifted into the second bidirectional shift register, and

when the select bit in the second control signals is in odd positions in the second bidirectional shift register, shifting the unselect signals into the first bidirectional shift register from the opposite direction of the one of the first and second directions in which the unselect signals are shifted into the second bidirectional shift register.

22. A method for selecting an output of a delay line comprising a plurality of taps, the plurality of taps including a plurality of sets of taps, comprising:

selecting in a first stage, selected taps from respective sets in the plurality of sets of taps;

selecting in a second stage, an output tap from the selected taps from the first stage; and

controlling the selecting in first stage and the selecting in the second stage selecting, for all pairs of adjacent taps in the plurality of taps, to change the output tap to the adjacent tap in the pair by switching in only one of the first stage or the second stage.